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a substrate having a circuit device;
a dielectric material overlying the circuit device with a via formed in the dielectric material to the circuit device, the via exposing a sidewall in the dielectric material and a surface of the circuit device;
a barrier material substantially lining the sidewall;
a seed layer on the barrier material and substantially lining the sidewall; and
a conductive material directly contacting the surface of the circuit device.

13. (Amended) The integrated circuit of claim 12, wherein the circuit device comprises an interconnection line.

14. (Amended) The integrated circuit of claim 12, wherein the conductive material is copper.

Please add the following claims:

15. (New) The integrated circuit of claim 12, wherein the barrier layer comprises an etch characteristic such that the barrier material can be selectively etched in the presence of the seed material.

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16. (New) An integrated circuit comprising:
a substrate having a circuit device;
a dielectric material overlying the circuit device with a via formed in the dielectric material to the circuit device, the via exposing a sidewall in the dielectric material and a surface of the circuit device;
a barrier material substantially lining the sidewall;
a seed layer on the barrier material and substantially lining the sidewall; and
a conductive material in the via;

wherein the seed layer and barrier material are formed so as to expose the circuit device at an end of the via.

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17. (New) The integrated circuit of claim 16, wherein the barrier layer comprises an etch characteristic such that the barrier material can be selectively etched in the presence of the seed material.
